AMENDMENTS TO THE CLAIMS

Claims 1-15 (Cancelled)

16. (New) An ESD protection circuit comprising:

a pad;

a to-be-protected circuit connected to the pad;

a MOS transistor having a drain, a source, and a gate; and

an npn bipolar junction transistor having a collector connected to the pad, an emitter connected to a ground line, and a base connected to the drain, only a single drain being connected to the base.

- 17. (New) The ESD protection circuit of claim 16 and further comprising a delay line having an input, and an output connected to the gate of the MOS transistor.
- 18. (New) The ESD protection circuit of claim 17 and further comprising a resistive device connected to the base and the ground line.
 - 19. (New) The ESD protection circuit of claim 17 and further comprising: a first resistive device connected to the base and the ground line; and a second resistive device connected to the gate and the ground line.
- 20. (New) The ESD protection circuit of claim 17 wherein the input of the delay line is connected to a power supply pad.
- 21. (New) The ESD protection circuit of claim 17 wherein the delay line has a delay period required for a signal to pass through the delay line, the delay period being greater than a period of an ESD event.

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22. (New) An ESD protection circuit comprising:

a pad;

a to-be-protected circuit connected to the pad;

an NMOS transistor having a drain, a source, and a gate; and

an npn bipolar junction transistor having a collector connected to the pad, an emitter connected to a ground line, and a base connected to the drain, no PMOS transistor being connected to the base.

- 23. (New) The ESD protection circuit of claim 22 and further comprising a delay line having an input, and an output connected to the gate of the NMOS transistor.
- 24. (New) The ESD protection circuit of claim 23 and further comprising a resistive device connected to the base and the ground line.
 - 25. (New) The ESD protection circuit of claim 23 and further comprising: a first resistive device connected to the base and the ground line; and a second resistive device connected to the gate and the ground line.
- 26. (New) The ESD protection circuit of claim 23 wherein the input of the delay line is connected to a power supply pad.
- 27. (New) The ESD protection circuit of claim 23 wherein the delay line has a delay period required for a signal to pass through the delay line, the delay period being greater than a period of an ESD event.

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